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(54) Title: THREE-DIMENSIONAL MEMORY ARRAY AND METHOD OF FABRICATION

(57) Abstract: A multi-level memory array is described employing rail-stacks. The rail-stacks include a conductor and semiconductor layers. The rail-stacks are generally separated by an insulating layer used to form antifuses. In one embodiment, one-half the diode is located in one rail-stack and the other half in the other rail-stack.

THREE-DIMENSIONAL MEMORY ARRAY AND METHOD OF FABRICATION

[0001] This is a continuation-in-part application of 09/560,626 filed 4/28/2000.

BACKGROUND OF THE INVENTION

1. Field of the Invention.

[0002] The invention relates to the field of vertically stacked field programmable non-volatile memory and method of fabrication.

2. Prior art.

[0003] Recently there has been an interest in fabricating memories having memory cells disposed at numerous levels above a substrate. Each level includes a plurality of spaced-apart first lines extending in one direction which are vertically separated from a plurality of parallel spaced-apart second lines in a second direction, for example, extending perpendicular to the first line. Cells are disposed between the first lines and second lines at the intersections of these lines. These memories are described in U.S. patents 5,835,396 and 6,034,882.

[0004] As will be seen, the present invention departs from the structures shown in these patents and uses "rail-stacks" as will be described later. The invented memory employs antifuses where a diode is formed upon programming a particular bit. In this connection see, *"A Novel High-Density Low-Cost Diode Programmable Read Only Memory,"* by de Graaf, Woerlee, Hart, Lifka, de Vreede, Janssen, Sluijs and Paulzen, IEDM-96, beginning at page 189 and U.S. patents 4,876,220; 4,881,114 and 4,543,594.

SUMMARY OF THE INVENTION

[0005] A multi-level memory array disposed above a substrate is disclosed. A first plurality of spaced-apart rail-stacks disposed at a first height and/or a first direction are fabricated above the substrate. Each rail-stack includes a first conductor and a first semiconductor layer extending substantially the entire length of the first conductor. A second plurality of spaced-apart rail-stacks are disposed above the first rail-stacks and run in a second direction different than the first direction. An insulating layer is formed

between the first rail-stack and the second conductors which is capable of being selectively breached by passing a current between one of the first and one of the second conductors to program the array.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is a perspective view of a cut-away portion of the invented array.

[0007] Figures 2A-2H illustrate some of the steps used to fabricate one embodiment of the invented memory.

[0008] Figure 2A is a cross-sectional elevation view of an antifuse and semiconductor layer formed during the fabrication of the invented array.

[0009] Figure 2B illustrates the structure of Figure 2A after an additional semiconductor layer has been formed.

[0010] Figure 2C illustrates the structure of Figure 2B after a conductive layer is formed.

[0011] Figure 2D illustrates the structure of Figure 2C after an additional semiconductor layer has been formed.

[0012] Figure 2E illustrates the structure of Figure 2D after a masking and etching step.

[0013] Figure 2F illustrates the structure of Figure 2E after open spaces left from the etching step have been filled.

[0014] Figure 2G illustrates the structure of Figure 2F after a planarization step.

[0015] Figure 2H illustrates the structure of Figure 2G after another antifuse layer is formed.

[0016] Figure 3 is a cross-sectional elevation view of one embodiment of the present invented array.

[0017] Figure 4 is a cross-sectional elevation view of a second embodiment of the invented array.

[0018] Figure 5 is a cross-sectional elevation view of a third embodiment of the invented array.

[0019] Figure 6 is a cross-sectional elevation view of another embodiment of the invented array.

[0020] Figure 7 is a cross-sectional elevation view of an embodiment employing rails.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0021] A three-dimensional memory array which is field programmable is described. In the following description, numerous specific details are set forth such as specific materials and layer thicknesses. It will be apparent, however, to one skilled in the art that the present invention may be practiced without these details. In other instances, well-known circuits and fabrication techniques have not been set forth in detail in order not to unnecessarily obscure the present invention.

OVERVIEW OF THE STRUCTURE OF THE INVENTED MEMORY ARRAY

[0022] The invented memory array is fabricated on several levels and, for instance, may have eight levels of storage. Each level includes partially or completely a first plurality of parallel spaced-apart rail-stacks running in a first direction and a second plurality of rail-stacks or conductors (depending on the embodiment) running in a second direction. A rail-stack may be shared by two levels of storage. Generally, the first rail-stacks run perpendicular to the second conductors/rail-stacks and hence form a right angle at their intersections.

[0023] The use of rail-stacks is a departure from prior art three-dimensional memories where conductors alone were used in lieu of rail-stacks, and where discrete cells (e.g., pillars) were formed at the intersections of the lines. As will be seen, a bit is stored at each of the intersections of rail-stacks. However, there is no apparent individual memory cell at the intersections, rather memory cells are defined by the rail-stacks and intermediate layers. This makes it easier to fabricate the invented array as will be seen. When the array is fabricated all the bits are in the zero (or one) state and after programming, the programmed bits are in the one (or zero) state.

[0024] In the embodiment of Figure 1, several rail-stacks are illustrated in the partial cross-section of the invented array. For instance, rail-stack 16 is shown at one height and a half rail-stack 18 is shown at a second height above the first height. Also, half rail-stacks are disposed between rail-stack 16 and a substrate 10. These lower half rail-stacks run in the same direction as the half rail-stack 18. A bit is stored at the intersection of rail-stacks and, for instance, a "cell" is present between the rail-stacks and layers shown

within the bracket 17 and another within the bracket 19. Each of these brackets span a memory level.

[0025] The array is fabricated on a substrate 10 which may be an ordinary monocrystaline silicon substrate. Decoding circuitry, sensing circuits, and programming circuits are fabricated in one embodiment within the substrate 10 under the memory array using, for instance, ordinary MOS fabrication techniques. (These circuits may also be fabricated above the substrate.) Vias are used to connect conductors within the rail-stacks to the substrate to allow access to each rail-stack in order to program data into the array and to read data from the array. For instance, the circuitry within the substrate 10 may select rail-stack 16 and the rail stack 18 in order to either program or read a bit associated with the intersection of these rail-stacks. (In the case of the embodiments of Figure 5 some conductors are not part of rail-stacks; these conductors are also coupled to the substrate circuits.)

[0026] As shown in Figure 1, an insulating layer 12 is formed over the substrate in order that the array may be fabricated above the substrate. This layer may be planarized with, for instance, chemical-mechanical polishing (CMP) to provide a flat surface upon which the array may be fabricated.

[0027] Following this, a conductive layer 14 is formed on the substrate. As will be seen, conductive layers are used within the rail-stacks and these layers and the resultant conductors may be fabricated from elemental metals such as tungsten, tantalum, aluminum, copper or metal alloys may be used such as MoW. Metal silicides may also be used such as $TiSi_2$, $CoSi_2$ or a conductive compound such as TiN, WC may be used. A highly doped semiconductor layer such as silicon is also suitable. Multiple layer structures may be used selecting one or more of the above.

[0028] Following the deposition of a conductive layer, a layer of semiconductor material (layer 15) such as silicon is formed over the conductive layer. This is typically a polysilicon layer; however, an amorphous layer may be used. Other semiconductor materials may be used such as Ge, GaAs, etc. In the embodiment of Figure 1 this semiconductor layer is highly doped and, as will be seen, forms one-half a diode. After masking and etching steps, half rail-stacks are formed. These rail-stacks are "half" or partial rail-stacks since they are approximately half the thickness of the rail-stacks used in subsequent levels.

[0029] Following this, in the embodiment of Figure 1, a material for the antifuses used to program the array is deposited shown as layer 20. In one embodiment, the layer 20 is a dielectric such as silicon dioxide which is deposited by chemical vapor deposition (CVD) in a blanket deposition over the half rail-stacks and over the dielectric fill, filling the space between the rail-stacks. In another embodiment the layer 20 is grown on the upper surface of the silicon layer 15 and only exists on the rail-stacks. Other materials that can be used for the anti-fuse layer are silicon dioxide, silicon nitride, silicon oxynitride, amorphous carbon or other insulating materials or combinations of materials. (Also an undoped layer of silicon may be used for the antifuse layer.)

[0030] Now a full set of memory array rail-stacks is formed on the layer 20. This comprises first the deposition of a lightly doped silicon layer 21 doped with a conductivity type dopant opposite to that used for the silicon layer 15, a heavily doped silicon layer 22 doped also opposite to the layer 15, a conductive layer 23 and a heavily doped silicon layer 24 doped with the same conductivity type dopant as layers 21 and 22. After masking and etching, the rail-stacks shown in Figure 1, such as rail-stack 16 are formed. These rail-stacks are, as illustrated, in a direction perpendicular to the rail-stacks above and below them.

[0031] While not shown in Figure 1 but as will be described later, the spaces between the rail-stacks after they are defined, are filled with a dielectric such as silicon dioxide. Then the rail-stacks and fill are planarized by CMP. In another embodiment spin-on-glass (SOG) is used to fill the voids. In this case chemical planarization can be used such as, for example, plasma etching. Other fill and planarization methods can be used.

[0032] After formation of the rail-stacks another antifuse layer 26 is formed, for instance, from a dielectric such as silicon dioxide.

[0033] Now another layer of rail-stacks are defined and only half rail-stacks are shown in Figure 1 at this upper level. This half rail-stack comprises a silicon layer 28 doped with a conductivity type dopant opposite to that of layer 24. This is a lightly doped layer. Another silicon layer 30 is formed on layer 28 and this layer is doped with the same conductivity type dopant as layer 28, however, it is more heavily doped. Then a conductive layer 31 is formed above the layer 30.

[0034] Half rail-stacks are used at the very upper-most level of the array and at the very lowest level of the array. In between the half rail-stacks a number of full rail-stacks, such as rail-stack 16, are used throughout the array.

[0035] It should be noted that the silicon layers disposed on the conductive layers extend the entire length of the rail-stacks in the embodiment of Figure 1 and are uninterrupted except possibly where vias are used to provide a conductive path to the substrate 10.

[0036] In Figure 1 a path 32 is illustrated from a lower conductor in level 17 to an upper conductor in this level found in the rail-stack 18. This path is accessed in one embodiment through decoding circuitry in the substrate for both programming and reading of data into and from the array for one bit.

[0037] For instance, to program the bit, a relatively high write voltage, 5-20V is applied between the conductors. This relatively high voltage causes a breach in the layer 26 creating a diode. Without this high voltage, the layer 26 remains an insulator. Thus, by selecting pairs of conductors, diodes can be selectively formed so as to program the array. It is currently performed that the write voltage be applied with a polarity such that the more positive voltage is applied to the rail-stack that constitutes the anode of the diode that is created by the breach of layer 21. It is also possible to program using a reverse-biasing potential.

[0038] To sense the data programmed into the array, a voltage lower than that for programming is used. This voltage is applied so as to forward-bias the diode of the cell being accessed and thus allowing a sense amplifier to determine whether or not the layer 26 is intact between the rail-stacks. Note that "sneak" or parasitic paths in the array which would interfere with the sensing will include a reverse-biased diode.

EMBODIMENT OF FIGURE 3

[0039] In the cross-section elevation view of Figure 3, one embodiment is illustrated which corresponds to the embodiment shown in Figure 1. In Figure 3 the half rail-stacks of Figure 1 are not illustrated. Three complete levels 35, 36 and 37 of the array are illustrated in Figure 3. Below layer 38 of Figure 3 other rail-stacks or half rail-stack are used. Also above layer 65, a full or half rail-stack is used.

[0040] The rail-stack 3 comprising layers 38 through 41 includes a lightly doped n- layer 38, a heavily doped n+ layer 39, a conductor layer 40 and n+ layer 41. The

fabrication of these rail-stacks will be discussed in more detail in conjunction with Figure 2A through Figure 2G. An antifuse layer 42 which for the embodiment of Figure 3 is a blanket deposition covers all of the rail-stacks formed below layer 42 as well as the fill filling the voids between the rails. As mentioned, the layer 42 is a deposited silicon dioxide layer in one embodiment.

[0041] It should be noted that n+ layers sandwich the conductor layer 40. These highly doped layers provide ohmic transitions to prevent unintended Schottky diode formation.

[0042] The layers above and below conductor 40 are not symmetrical for the embodiment illustrated in that an n- layer 38 is used below the conductor 40 and not above the conductor 40. Only a single lightly doped layer (in conjunction with a heavily doped layer) is needed to define a diode; the thickness of this lightly doped layer is important in controlling the break-down voltage and resistance of the diode so formed. The layer 41, a heavily doped semiconductor layer, and the fill are planarized after the rail-stacks are defined and then a blanket deposition of the antifuse layer 42 is formed on the layer 41. (The lines 43 in Figure 3 are used to indicate that the antifuse layer 42 and like layers are not etched with the rail-stack below it and thus extend over the entire array for the illustrated embodiment.)

[0043] One advantage to the layer 42 and the other like layers in the structure, such as layers 51, 56 and 65, is that since they are an unbroken deposition, sidewall leakage (into the rail-stacks below) will be minimized, limiting electrical problems during reading and writing. When subsequent conductive material is deposited, it is unable to reach the sides of the rail-stacks below it because of this blanket deposition of the antifuse layer. For instance, path 49 which would allow silicon from layer 52 to cause a parasitic path does not exist because of the unbroken blanket deposition of the antifuse layer 51.

[0044] Rail-stacks 4 comprising layers 44, 45, 46 and 47 are formed on the antifuse layer 42. Layer 44 is lightly doped with a p-type dopant for the embodiment illustrated followed by a p+ layer 45, a conductive layer 46 and a p+ layer 47. After these layers are deposited, they are masked and etched to define the rail-stacks. Then the voids between these rail-stacks, such as void 50, are filled with a dielectric. The fill dielectric is planarized along with a portion of p+ layer 47. Planarization is done at this point in the fabrication since there is generally poor control over the thickness and

contour of the fill. The fill tends to build up on the rail-stacks when a non-spin-on type deposition is used. This is followed by a blanket deposition of layer 51.

[0045] The process is now repeated this time beginning with an n- layer 52 followed by an n+ layer 53, a conductive layer 54 and n+ layer 55. Again after defining the rail-stacks 5, the voids are filled and the surface is planarized. Another antifuse layer 56 is deposited.

[0046] The process is repeated for the rail-stacks 6 this time beginning with a p- layer 61, p+ layer 62, conductive layer 63, p+ layer 64. Again after defining the rail-stacks, filling the void 60 and then planarizing, another antifuse layer 65 is deposited.

[0047] As shown by the path 66, when a large enough voltage is applied between conductors 46 and 54, the antifuse layer 51, at the intersection of layers 47 and 52, is breached creating a diode at the intersection. As mentioned, this is selectively done throughout the array to program the array. The conductor 54 is therefore a bit line for the "cells" above and below it, for instance path 67 indicates another possible current path for another "cell" where the conductor 54 is again a bit line during sensing.

[0048] It should be noted that with the reversal of the p- and n- layers at each successive rail-stack, planarization for this embodiment always occurs on a heavily doped layer such as layer 47 and layer 55. Moreover, the lightly doped layers are always formed on relatively planar surfaces, consequently their thickness can be more easily controlled. This, as mentioned, allows the characteristics of the diode (once the intermediate antifuse layer is breached) to be more reliably controlled.

PROCESSING FLOW FOR THE EMBODIMENT OF FIGURE 3

[0049] The process flow for forming rail-stack 5 of Figure 3 is illustrated in Figures 2A-2H. It will be apparent that the rail-stacks for the other embodiment (Figures 4 and 5) are similarly processed.

[0050] First, as shown in Figure 2A an antifuse layer 51 is deposited. This typically is 50-200Å of silicon dioxide which can be deposited with any one of very well-known processes. Following this, a silicon layer 52 is deposited which is typically 1000-4000Å thick and formed with a CVD process where a phosphorous dopant is deposited along with the deposition of for instance, the polysilicon semiconductor material or where the dopant is ion implanted following the deposition of the layer. This layer is doped to a level of, for example, $1x10^{17}$ /cm^3, but can be doped to a level in a range from $1x10^{15}$ /cm^3 to $1x10^{19}$ /cm^3.

[0051] Now, as shown in Figure 2B, an n+ layer 53 is deposited again using CVD. This layer may be approximately 300-3000Å thick and in one embodiment is doped to a level of $>10^{19}$/cm^3.

[0052] Throughout this application two adjacent silicon layers are often shown such as layers 52 and 53, with different doping. These layers may be formed with one deposition and using ion implantation steps at two different energy levels to obtain the two doping levels. Also, these differently doped layers may be formed by introducing different amounts of dopant in a diffusion process as a layer is formed.

[0053] A conductive layer which may be 500-1500Å thick is formed using any one of numerous well-known thin film deposition process such as sputtering. A refractory metal may be used or a silicide of a refractory metal. Also as mentioned aluminum or copper can be used, or more simply the heavily doped silicon can be the conductor. In one embodiment, Ti and TiN layers are formed on the silicon layer and the wafer is heated to form a silicide. For instance, a Ti layer of 250Å and a TiN layer of 70Å are heated at 600°C for one minute to form the silicide.

[0054] Next another semiconductor layer of, for instance, polysilicon approximately 1500-2000Å thick is formed again doped to a level of $>10^{19}$/cm^3. This is shown as layer 55 in Figure 2D; after planarization its thickness is between 300Å and 2000Å thick.

[0055] A masking and etching step is now used to define rail-stacks, such as rail-stacks 69, 70 and 71 shown in Figure 2E. Note that when comparing this view to the view of

rail-stack 5 of Figure 3, the view in Figure 2E is taken from the side and consequently shows the individual rail-stacks. An ordinary masking and etching step for instance using plasma etching, may be used. Etchants can be used that stop on the antifuse layer thus preventing this layer from being etched away. Thus, layer 51 can be considered an etchant stop layer depending on the specific etchants used.

[0056] Now as shown in Figure 2F, the spaces between the rail-stacks are filled with a dielectric such as formed with a HDPCVD process.

[0057] Chemical-mechanical polishing is then employed to planarize the upper surface of the rail-stacks shown in Figure 2F in one embodiment. Chemical etching can also be used as mentioned with certain dielectrics. This planarization can reduce the thickness of the layer 55 to approximately 500Å, thus this layer ends up being of approximately the same thickness as the layer 53.

[0058] Next as shown in Figure 2H another antifuse layer 56 is formed on the planarized surface 75. Since the layer 56 is deposited over all the rail-stacks and the filler material and remains unetched, it forms a barrier to the migration of the materials subsequently deposited that might make their way along the sides of the rail-stacks such as along path 79. Thus the layer 56 helps prevent the parasitic paths and potential shorts that may occur with prior art memories.

[0059] It should be noted that in Figure 3 while the antifuse layer is shown as a blanket layer covering the rail-stacks and fill, it is possible also to fabricate each level where the antifuse layer is in fact grown from a semiconductor layer. For instance, an oxidation step may be used to grow a silicon dioxide layer from layers 41, 47, 55 and 64. This grown layer would then be in lieu of the antifuse layers shown in Figure 3.

[0060] In all the embodiments, the rail-stacks and rails for the embodiment of Figure 7 are connected to circuitry in the substrate such as decoders, sense amps and like peripheral circuits. Vias for providing these connections are discussed in co-pending application number 09,746,341, entitled "Contact and Via Structure and Method of Fabrication."

THE EMBODIMENT OF FIGURE 4

[0061] For the embodiment of Figure 4 each rail-stack begins with a conductor such as layer 80 of Figure 4. An n+ semiconductor layer 81 and an n- layer 82 are formed on layer 80. Next a layer of antifuse material 83 is formed. Then a p+ layer 84 of

semiconductor material is deposited (e.g., silicon with boron dopant) on the antifuse. When the rail-stacks are formed, for instance for rail-stack 2 of Figure 4, the antifuse layer 83 is etched as well as layers 80, 81, 82 and 84.

[0062] The voids between the rail stacks are now filled and planarization is done, planarizing the fill with the upper surface of the layer 84. Following the completion of the rail-stack 2 the next rail-stacks are formed shown as rail-stacks 3 in Figure 4. This comprises a conductor layer 85, p+ layer 86, p- layer 87, antifuse layer 88 and n+ layer 89. Again masking and etching occur. This etching also etches the exposed regions of layer 84 which does not appear in the view of Figure 4, but this will be apparent shortly when region 95 of the next stack is discussed. Now filling and planarization occurs and the next layer of rail-stacks are formed shown as rail-stack 4. As illustrated, this comprises a conductive layer 90, n+ layer 91, n- layer 92, antifuse layer 93, and p+ layer 94. Once again masking, etching, filling and planarization occur.

[0063] Unlike the embodiment of Figure 3, when rail-stacks at any particular height are formed, etching must occur on one layer of the rail-stack immediately below the rail-stack being defined. For instance, when rail-stack 4 is etched the layer 89 of rail-stack 3 is etched away where it is not covered by rail-stack 4 as shown by region 95. This etching is used to remove all of the semiconductor material between the adjacent conductors and consequently prevent a path, such as path 96 shown in Figure 4. This etching also occurs to layer 84 which, as mentioned, is not seen in Figure 4. In this connection the antifuse layer 88 can be used as an etchant stop, although this is not necessary. No harm is done if etching does occur through the layer 88 since the antifuse layer is only needed at the intersections of the rail-stacks. Note the etching of the region 95 is done in alignment with overlying rail-stacks and consequently no additional masking is required.

[0064] As was the case with the earlier embodiment, the order of the n and p doped layers alternate with each successive rail-stack. Moreover, the rail-stacks at any given level include both p and n layers. In contrast, for the embodiment of Figure 3, at any particular level, the rail-stacks are doped with either an n type or p type dopant but not both.

EMBODIMENT OF FIGURE 5

[0065] In the embodiment of Figure 5, alternate levels of rail-stacks running in a first direction and intermediate layers of conductors are running in a second direction are used. For instance as shown in Figure 5, the conductors 3, 5 and 7 run in a first direction whereas the rail-stacks 4 and 6 run in a second direction.

[0066] In this embodiment each of the rail-stacks is symmetrical about a conductor such as conductor 109 of rail-stack 4. The conductor is sandwiched between two n+ layers 108 and 110. More lightly doped outer layers 107 and 111 are disposed on these more heavily doped layers.

[0067] In fabrication the conductors such as conductors 105, are first formed, for instance, on the substrate. The spaces between these conductors may be filled and planarization may occur. Then an antifuse layer 106, n- layer 107, n+ layer 108, conductive layer 109, n+ layer 110 and n- layer 111 are deposited. Rail-stacks are then defined by masking and etching. The voids between the rail-stacks are then filled with a dielectric. Then planarization of the filling material and the upper surface of layer 111 is performed. Following this, antifuse layer 112 is deposited over the entire array. Now additional conductors are formed such as conductors 113. Each level in this array is between a metallic conductor such as conductor 105, and a sandwich conductor such as conductor 109. Thus there are four memory levels shown in Figure 5, levels 100, 101, 102 and 103.

[0068] Programming in this array causes the formation of Schottky diodes. Consequently, the conductors such as conductors 105 and 113 must be of a suitable material to allow formation of a Schottky diode. For instance, aluminum and some refractory metal or silicides may be used.

EMBODIMENTS WITH SINGLE TYPE PN DIODES

[0069] Some of the embodiments discussed above use both p-n+ and p+n- diode types. In some processes, one of these diode types may exhibit more leakage than the other. Consequently, it may be desirable to have, for these processes, an array with only a single diode type. More specifically, assume a process has higher leakage for diodes which are p-n+ type than the same process has for diodes of the p+n- type. Figure 6 illustrates an array embodiment where, if the antifuse layer is breached, all the diodes will be p+n- type, that is, there will be no diodes with a p-n+ junction.

[0070] In Figure 6, three rail-stacks 120, 121, and 122 are illustrated which will create only a single type diode specifically, p+n-. The first rail-stack 120 comprises: a p+ semiconductor layer 25 of, for instance, 1,000Å thick; a conductor 126 of, for example, 500Å thick; a p+ layer 127 of, for example, 1,000Å thick; and a anti-fuse layer 128 of approximately 30Å thick. These layers may be formed as discussed above. Rail-stack 121 comprises: an n- semiconductor layer 129 of, for instance, 2,000Å thick; an n+ semiconductor layer 130 of, for example, 500Å thick; a conductor 131 of, for instance, 500Å thick; an n+ semiconductor layer 132 of, for instance, 500Å thick; and an n- semiconductor layer 133 of, for example, 2,000Å thick. The rail-stack 122 has the same layering as the rail-stack 120.

[0071] As discussed above, the semiconductor layers may be formed using polysilicon or an amorphous silicon. The conductors may be a highly doped silicon or a metal, metal alloy, silicide or combinations thereof. The dielectric fill in the spaces between the rail-stacks is also used as discussed for the earlier embodiments.

[0072] As can be seen from Figure 6, if the antifuse layer is breached, the diodes between the conductors 126 and 131 are all p+n- type, and similarly, the diodes in the next level between the conductors 131 and 140 are again all p+n- type. The rail-stacks shown are used throughout the memory array so that the entire array has only p+n- type diodes in its memory cells.

[0073] The diodes in the illustrated rail-stacks of Figure 6 are forward biased towards the conductor 131 and the conductor 141. If need be for a particular application, the diodes can be oriented identically, that is, with all their anodes (or cathodes) pointing upwardly. This can be obtained for the p+n- type diodes by having both a p+ doped and n- doped semiconductor layer in each of the rail-stacks. For instance, layer 132 and 133 would be replaced with a p+ layer and layer 142 would be replaced with n- and n+ layers. This still maintains only one type of diode (p+n-) throughout the array.

[0074] While Figure 6 shows that after the antifuse is breached, only p+n diodes will be created, an array with only p-n+ type diodes can be fabricated by replacing the p+ layers with an n+ layer and replacing the n+ and n- layers with p+ and p- layers. Also, the array can have the anodes (or cathodes) vertically aligned as discussed above for the p+n- type diodes.

[0075] It should be noted that for the embodiment of Figure 6, planarization occurs on an n- layer, for example, the n- layer 133 is planarized before the formation of the anti-fuse layer. For this reason, layer 133 is somewhat thicker. More care is required in the polishing of the n- layer 133 to assure uniformity across the wafer and the resultant uniform diode characteristics. In this connection, a "hard" mask may be used such as described in co-pending application serial number 09/746,469, filed by N. Johan Knall and James M. Cleeves, and titled *Methods Of Forming Nonvolatile Memory Devices Utilizing A Hard Mask* assigned to the assignee of the present application. One result of having thicker n- layers is that the rail-stack 121 is thicker than the rail-stacks 120 and 122.

[0076] Another array embodiment which results in single type diode junction is shown in Figure 7. This embodiment employs rails of a uniformly doped semiconductor material rather than the rail-stacks previously discussed, which comprise layers. More specifically, as shown in Figure 7, rails 150 of, for example, a polysilicon doped with a p- type dopant are defined from a layer of polysilicon. The spaces between these rails, as previously done with the rail-stacks, are filled with a dielectric. Then planarization occurs. An anti-fuse layer 154 is grown on, or deposited onto, the rails 150.

[0077] Now, an n- type polysilicon layer is formed and orthogonal rails 151 and 152 are photolithographically formed. Then, following a filling step, and a planarization step, another anti-fuse layer 153 is formed. Next, p- type polysilicon rails 156 are formed and an anti-fuse layer 155 is formed on these rails as shown in Figure 7.

[0078] Each of the polysilicon rails or lines 150, 151, 152, and 156 and like lines at other levels are connected to circuitry in a substrate. Each of the rails is both a conductor and one-half a diode for cells. For instance, a cell is formed between rail 156 and rail 151, and another cell between rail 156 and rail 152. Likewise, cells are formed between the rail 150 and each of the rails 151 and 152.

[0079] The advantage to the embodiment of Figure 7 is its ease of fabrication.

[0080] Typically, the semiconductor rails are less conductive than metal conductors previously discussed, and consequently, the rails will have more resistance. This for instance, will increase the access time of the cells, particularly in a large array. The conductivity of the rails can be improved by increasing the concentration of the p type and n type dopants. However, when this is done, the leakage current increases. For any

given array, decreased resistance can be traded-off for increased leakage and vice-versa. It is contemplated that this embodiment will typically be used in a relatively small array where high-speed access is not critical.

[0081] As can be seen from Figure 7, after the antifuse is breached, the diodes associated with each of the cells are the same; specifically the p and n type dopant concentrations for each diode is the same.

OTHER EMBODIMENTS

[0082] In the above description a conductor is shared by two levels. An array may be fabricated where there are two conductors for each level that are not shared with other levels. A dielectric may be used to separate each such level. Also while above diodes on alternate levels "point" in the same direction for some embodiments, this is not necessary. For instance, a shared conductor may have diodes point-in from above and point-out from below. This requires different driving circuitry in the substrate.

[0083] All the above embodiment have benefits over the prior art three-dimensional memories. One advantage is that the diodes are formed by breaching an antifuse layer. This results in diodes with very small junction areas. The resultant low-leakage diodes improves the performance of the array. Additionally, etching is not as deep as with the prior art three-dimensional memories. Difficulties with stringers where individual pillars were used in the prior art is eliminated with some of the above embodiments. The different embodiments provide numerous material choices and "post-write diode" choices.

[0084] Thus a three-dimensional memory array has been described using rail-stacks (and for one embodiment rails) which simplifies processing and provides better performance over prior art three-dimensional arrays.

CLAIMS:

What is claimed is:

1. A memory array disposed above a substrate comprising:

a first plurality of spaced-apart rail-stacks disposed at a first height in a first direction above the substrate, each rail-stack including a first conductor and a first semiconductor layer extending substantially the entire length of the first conductor;

a second plurality of spaced-apart conductors disposed above the first height and in a second direction different than the first direction, and

an insulating layer disposed between the first rail-stack and the second conductors which is capable of being selectively breached by passing a current between one of the first and one of the second conductors to program the array.

2. The array defined by claim 1 wherein the first semiconductor layer is a silicon layer.

3. The array defined by claim 2 wherein the first and second conductors are perpendicular to one another.

4. The array defined by claim 3 wherein the first silicon layer is more heavily doped adjacent to the first conductor than it is at its surface spaced-apart from the first conductor.

5. The array defined by claim 4 wherein the second conductors have a second silicon layer disposed on the second conductors extending substantially the entire length of the second conductors.

6. The array defined by claim 4 wherein the insulating layer is on the surface of the first silicon layer spaced-apart from the first conductor.

7. The array defined by claim 6 wherein the second conductors are on the insulating layer.

8. The array defined by claim 7 wherein the silicon is doped with an n-type dopant.

9. The array defined by claim 8 wherein Schottky diodes are formed to program the array.

10. The array defined by claim1 wherein the insulating layer is substantially continuous between the first plurality of rail-stacks and the second plurality of conductors.

11. The array defined by claim 1 wherein the insulating layer provides a physical barrier between the first plurality of rail-stacks and the second plurality of conductors.

12. A memory array disposed above a substrate comprising:

a first plurality of parallel spaced-apart rail-stacks disposed above the substrate running in a first direction;

a second plurality of parallel spaced-apart rail-stacks disposed above the first rail-stacks, the second plurality of rail-stacks running in a second direction different than the first direction such that a projection of the second rail-stack on the first rail-stack define intersections with the first plurality of rail-stacks; and

a layer of low conducting material separating the first plurality of rail-stacks from the second plurality of rail-stacks, the layer of low conducting material at each intersection of the first and second rail-stacks separating a first conductivity type doped semiconductor material in one of the first rail-stacks from a second conductivity type doped semiconductor material in one of the second rail-stacks.

13. The memory array defined by claim 12 wherein the semiconductor material is silicon.

14. The memory array defined by claim 12 wherein the layer of low conducting material provides a physical barrier between the first and second plurality of rail-stacks, substantially minimizing sidewall leakage.

15. The memory array defined by claim 13 wherein the passage of a current equal to or greater than a predetermined threshold from one of the first rail-stacks to one of the second rail-stacks causes a diode to form at the intersection of these rail-stacks.

16. The memory array defined by claim 15 wherein the silicon on one side of each intersection is more lightly doped than the silicon on the opposite side of each intersection.

17. The memory array defined by claim 16 wherein the side of the intersection having the more lightly doped silicon includes a more heavily doped silicon region between the more lightly doped silicon and its respective conductor.

18. The memory array defined by claims 11 or 17 wherein the low conducting material comprises silicon dioxide.

19. The memory array defined by claims 11 or 17 wherein the low conducting material layer comprises silicon nitride.

20. The memory array defined by claims 11 or 17 wherein the low conducting material layer comprises undoped silicon.

21. The memory array defined by claims 11 or 17 wherein the first and second rail-stacks include a conductor comprising a metal or a metallic compound.

22. The memory array defined by claim 21 wherein each conductor is sandwiched between silicon in a multi-level array.

23. The memory array defined by claim 12 wherein the layer of low conductivity material is grown from a semiconductor layer.

24. In a multi-level memory having alternate levels of first spaced-apart conductors extending in one direction and second spaced-apart conductors in the other levels extending in a second direction, an improvement wherein each first conductor includes:

a first layer of a first conductivity type doped semiconductor material disposed on one side of the conductor over substantially its entire length;

a second layer of the first conductivity type doped semiconductor material disposed on the opposite side of the conductor over substantially its entire length;

a third layer of the first conductivity type doped semiconductor material disposed on the second layer over substantially its entire length, the third layer being more lightly doped than the second layer; and

a dielectric disposed on the third layer.

25. The memory defined by claim 24 wherein the semiconductor material is silicon.

26. The memory defined by claim 25 wherein the dielectric is grown from the semiconductor material.

27. The memory defined by claim 26 wherein the dielectric is silicon dioxide.

28. The memory defined by claim 25 wherein the dielectric is silicon nitride.

29. The memory defined by claim 25 wherein the dielectric extends substantially continuously between the levels.

30. The memory defined by claim 24 wherein the memory is programmed by forming Schottky diodes at selected intersections of the first and second conductors.

31. The memory defined by claims 24 or 25 wherein a second dielectric is disposed on the first layer.

32. The memory defined by claim 24 wherein each second conductor includes:

a fourth layer of a second conductivity type doped semiconductor material disposed on one side of the second conductor over substantially its entire length;

a fifth layer of a second conductivity type doped semiconductor material disposed on the opposite side of the second conductor over substantially its entire length;

a sixth layer of the second conductivity type doped semiconductor material disposed on the fifth layer over substantially its entire length, the sixth layer being more lightly doped than the fifth layer; and

a third dielectric disposed on the sixth layer.

33. The memory defined by claim 32 wherein the second conductivity type doped material is doped silicon.

34. In a multi-level memory having alternate levels of first spaced-apart conductors extending in one direction and second spaced-apart conductors in the other levels extending in a second direction, an improvement wherein each first conductor includes:

a first layer of a first conductivity type doped semiconductor material disposed on one side of the first conductor over substantially its entire length;

a second layer of the first conductivity type doped semiconductor material disposed on the first layer over substantially its entire length, the second layer being more lightly doped than the first layer; and

a first dielectric layer disposed on the second layer.

35. The memory defined by claim 34 wherein the semiconductor material is silicon.

36. The memory of claim 35 wherein the second conductors include:

a third layer of silicon doped with a second conductivity type dopant extending over substantially its entire length; and

a second dielectric layer disposed on the third layer.

37. The memory defined by claim 34 wherein additional silicon layers are disposed on the first and second dielectric.

38. The array defined by claim 34 wherein p+n- diodes are formed at all levels of the array where programming occurs.

39. The array defined by claim 34 wherein p-n+ diodes are formed at all levels of the array where programming occurs.

40. The memory defined by claim 38 wherein the first dielectric layer at each level is silicon dioxide.

41. The memory defined by claim 40 wherein each dielectric layer is substantially continuous at each level.

42. The memory defined by claim 40 wherein the dielectric layer is grown from silicon.

43. The memory defined by claim 41 wherein the dielectric layer is blanket deposited.

44. The memory defined by claim 38 or 39 wherein the first dielectric layer at each level is silicon nitride.

45. A multi-level non-volatile memory array comprising:

a plurality of first rail-stacks disposed at a first and third level running generally in a first direction above a substrate, each rail-stack comprising first conductors sandwiched between layers of silicon;

a plurality of second rail-stacks disposed at a second and fourth level above the substrate and running in a second direction, each of the second rail-stacks comprising second conductors sandwiched between layers of silicon, and

a plurality of layers of dielectric each disposed respectively between successive levels of the first and second rail-stacks which are capable of being selectively breached to program the array.

46. The array defined by claim 45 wherein the layers of silicon on the first conductors are doped with a first conductivity type dopant and wherein the layers of silicon on the second conductor are doped with a second conductivity type dopant.

47. The array defined by claim 45 wherein the layers of dielectric are blanket deposited.

48. The array defined by claim 45 wherein the layers of dielectric are grown on the silicon.

49. The array defined by claim 45 where the layers of dielectric are substantially continuous, forming a physical barrier between levels of rail-stacks.

50. The array defined by claim 45 wherein the layers of silicon on at least one side of the first conductors are more heavily doped adjacent to the first conductor than they are further from the first conductor.

51. The array defined by claim 50 wherein p+n- diodes are formed at all levels of the array where programming occurs.

52. The array defined by claim 38 wherein p-n+ diodes are formed at all levels of the array where programming occurs.

53. The array defined by claim 46 wherein the layers of silicon on at least one side of the second conductors are more heavily doped adjacent to the second conductors than they are further from the second conductors.

54. The array defined by claim 50, 52, or 53 wherein the layer of dielectric comprises silicon dioxide.

55. The array defined by claim 50, 52, or 53 wherein the layer of dielectric comprises silicon nitride.

56. The array defined by claim 50 or 52 wherein the first rail-stacks and second rail-stacks form right angles.

57. A multi-level non-volatile memory array comprising:

a plurality of first rail-stacks disposed at a first and third level running generally in a first direction above a substrate, each rail-stack comprising first conductors sandwiched between layers of silicon;

a plurality of second rail-stacks disposed at a second and fourth level above the substrate and running in a second direction, each of the second rail-stacks comprising second conductors sandwiched between layers of silicon, and

a plurality of dielectric regions disposed between levels of the first and second rail-stacks which are capable of being selectively breached to program the array.

58. The array defined by claim 57 wherein the dielectric regions are grown from one of the layers of silicon.

59. The array defined by claims 57 or 58 wherein p-n+ diodes are formed between each of the first and second rail-stacks where programming occurs.

60. The array defined by claim 57 or 58 wherein p+n- diodes are formed between each of the first and second rail-stacks where programming occurs.

61. In a multi-level memory having alternate levels of first spaced-apart conductors extending in one direction and second spaced-apart conductors in the other levels extending in a second direction, an improvement wherein each of the first conductors includes:

a first layer of a first conductivity type doped semiconductor material disposed on one side of the first conductor over substantially its entire length;

a second layer of the first conductivity type doped semiconductor material disposed on the opposite side of the first conductor over substantially its entire length;

a third layer of the first conductivity type doped semiconductor material disposed on the first layer over substantially its entire length, the third layer being more lightly doped than the first layer;

a fourth layer of the first conductivity type doped semiconductor material disposed on the second layer over substantially its entire length, the fourth layer being more lightly doped than the second layer;

a first dielectric layer disposed on the third layer.

62. The memory of claim 61 wherein the dielectric layer is formed on the third layer by blanket deposition.

63. The memory of claim 61 wherein the dielectric layer is grown on the third layer.

64. The memory of claim 61 wherein the dielectric layer is substantially continuous over and at least two spaced-apart conductors extending in the one direction at least two spaced-apart conductors extending in the second direction.

65. The memory defined by claim 61 wherein each second conductor includes:

a fifth layer of a second conductivity type doped material disposed on one side of the second conductor over substantially its entire length;

a sixth layer of the second conductivity type doped material disposed on the opposite side of the second conductor over substantially its entire length;

a second dielectric layer disposed on the sixth layer.

66. The memory defined by claims 61 or 65 where the projection of the intersection of the first and second conductors at each level defines a p+n- diode.

67. The memory defined in claims 61 or 65 wherein at the projection of the intersection of the first and second conductors at each level defines a p+n- diode.

68. The memory defined by claim 61 wherein the semiconductor material is silicon.

69. The memory defined by claim 63 which the semiconductor material is silicon.

70. The memory defined by claim 68 wherein the dielectric of silicon dioxide.

71. The memory defined by claim 69 wherein the dielectric is silicon nitride.

72. A three dimensional memory array comprising:

a plurality of first spaced-apart parallel semiconductor rails doped with a first conductivity type dopant the first rack being disposed in a first direction and disposed at even levels in the array;

a plurality of second spaced-apart parallel semiconductor rails doped with a second conductivity type dopant, the second rail being disposed in a second direction different from the first direction and disposed as odd levels in the array; and

an anti-fuse layer separating at least the intersections of the first and second rails at each level.

73. The array defined by claim 72 wherein the first semiconductor rails are uniformly doped silicon rails.

74. The array defined by claim 73 wherein the second semiconductor rails are uniformly doped silicon rails.

75. The array defined by claim 72 wherein the antifuse layer is substantially continuous across the array.

76. The array defined by claims 73 or 74 wherein the antifuse material is a grown silicon dioxide layer.

77. The array defined by claims 72 or 74 wherein the antifuse material is a deposited silicon dioxide layer.

78. The array defined by claim 72 or 74 wherein the antifuse material is silicon nitride.

79. The array defined by claim 72 or 74 wherein the array is fabricated on a semiconductor substrate and each of the rails is coupled to circuitry in the substrate.

80. A multi-level non-volatile memory array comprising:

a plurality of first rail-stacks disposed at a first and third level running generally in a first direction above a substrate, each rail-stack comprising first conductors sandwiched between layers of silicon;

a plurality of second rail-stacks being thicker than the first rail-stack, disposed at a second and fourth level above the substrate and running in a second direction, each of the second rail-stacks comprising second conductors sandwiched between layers of silicon, and

a plurality of layers of dielectric each disposed respectively between successive levels of the first and second rail-stacks which are capable of being selectively breached to program the array.

81. The array defined by claim 80 wherein the layers of silicon on the first conductors are doped with a first conductivity type dopant and wherein the layers of silicon on the second conductor are doped with a second conductivity type dopant.

82. The array defined by claim 81 wherein the layers of silicon on at least one side of the first conductors are more heavily doped adjacent to the first conductor than they are further from the first conductor.

83. The array defined by claim 80 wherein p+n- diodes are formed at all levels of the array where programming occurs.

84. The array defined by claim 80 wherein p-n+ diodes are formed at all levels of the array where programming occurs.

85. The array defined by claims 80, 83, or 84 wherein the layer of dielectric comprises silicon dioxide.

86. The array defined by claim 80, 83, or 84 wherein the layer of dielectric comprises silicon nitride.

87. The array defined by claim 80, 83, or 84 wherein the first rail-stacks and second rail-stacks form right angles.

88. A method for fabricating a multi-level memory array comprising the steps of:

depositing a metal layer;

forming at least one layer of silicon on the metal layer where the silicon is doped with a first conductivity type dopant;

masking and etching the silicon and metal layers to define a plurality of parallel, spaced-apart rail-stacks;

filling the space between the rail-stacks with a dielectric material;

planarizing the silicon layer and the dielectric material to form a planarized surface, and

forming a layer of material for an antifuse on the planarized surface.

89. The method defined by claim 88 wherein the layer of antifuse material comprises a dielectric.

90. The method defined by claim 88 wherein the layer of antifuse metal comprises undoped silicon.

91. The method defined by claim 88 wherein the layer of antifuse material is grown on the rail-stacks.

92. The method defined by claim 88 wherein the layer of antifuse material is a blanket deposition on the rail-stacks and filling material.

93. The method defined by claim 89 wherein the silicon layer comprises a first silicon heavily doped with an n-type dopant and a second layer more lightly doped with the n-type dopant.

94. The method defined by claim 89 wherein the silicon layer is a heavily doped layer.

95. The method defined by claim 94 wherein the antifuse layer is approximately 80-200Å thick and comprises silicon dioxide.

96. A method for fabricating a multi-level memory array comprising the steps of:

forming a metal layer;

forming a first silicon layer heavily doped with a first conductivity type dopant on the metal layer;

depositing a second silicon layer on the first silicon layer, the second silicon layer being more lightly doped than the first layer with the first conductivity type dopant;

forming a layer of an antifuse material on the second silicon layer;

depositing a third silicon layer on the layer of antifuse material heavily doped with a second conductivity type dopant;

defining spaced-apart rail-stacks from the conductive layer, first and second silicon layers, the layer of antifuse material and third silicon layer;

filling space between the rail-stacks with a dielectric, and

planarizing the upper surface of the dielectric fill and the third silicon layer.

97. The method of claim 96 including repeating the steps of claim 49 to form second lines disposed above the first lines and generally perpendicular to the first lines.

98. The method defined by claim 97 including additionally etching through the third silicon layer of the first lines in alignment with the second lines.

99. A method for fabricating a multi-level memory array comprising the steps of:

forming a conductor layer;

forming a first silicon layer doped with a first conductivity type dopant on the conductive layer;

forming a second silicon layer on the first silicon layer, the second silicon layer being more lightly doped than the first layer with the first conductivity type dopant;

forming a layer of an antifuse material on the second silicon layer;

forming a third silicon layer on the layer of antifuse material doped with a second conductivity type dopant;

defining spaced-apart first rail-stacks from the conductive layer, the first and second silicon layers, the layer of antifuse material and the third silicon layer;

filling between the first rail-stacks with a dielectric, and

planarizing the upper surface of the dielectric fill and the third silicon layer.

100. The method defined by claim 99 wherein the layer of antifuse material is an oxide grown on the second silicon layer.

101. The method defined by claim 100 wherein the layer of antifuse material is a deposited dielectric.

102. The method of claim 99 including repeating the steps of claim 75 to form second rail-stacks disposed above the first rail-stacks perpendicular to the first rail-stacks.

103. The method defined by claim 102 including additionally etching through the third silicon layer of the first rail-stacks in alignment with the second rail-stacks.

104. A method for fabricating a multi-level memory array comprising the steps of:

forming a first silicon layer lightly doped with a first conductivity type dopant;

forming a second silicon layer more heavily doped than the first layer with the first conductivity type dopant;

depositing a conductive layer on the second silicon layer;

depositing a third silicon layer heavily doped with a second conductivity type dopant;

etching the first, second and third silicon layers and conductive layers to define a plurality of parallel, spaced-apart rail-stacks;

filling the space between the rail-stacks with a dielectric material;

planarizing the third silicon layer and the dielectric filling material, and

depositing a layer of an antifuse material on the planarized surface.

105. The method defined by claim 104 wherein the conductive layer is approximately 500-1,500Å thick.

106. The method defined in claim 104 wherein the first silicon layer is 1000-4000Å thick.

107. The method defined in claim 102 wherein the second silicon layer is approximately 300-3000Å thick.

108. The method defined in claim 102 wherein the third silicon layer is approximately 300-2000Å thick after planarization.

109. The method defined by claim 102 wherein the antifuse layer is a silicon dioxide layer with a thickness of approximately <200Å thick.

110. The method defined by claim 102 wherein the antifuse layer is a grown silicon dioxide layer grown from the third silicon layer.

111. The method defined by claim 102 wherein the antifuse layer is a silicon nitride layer.

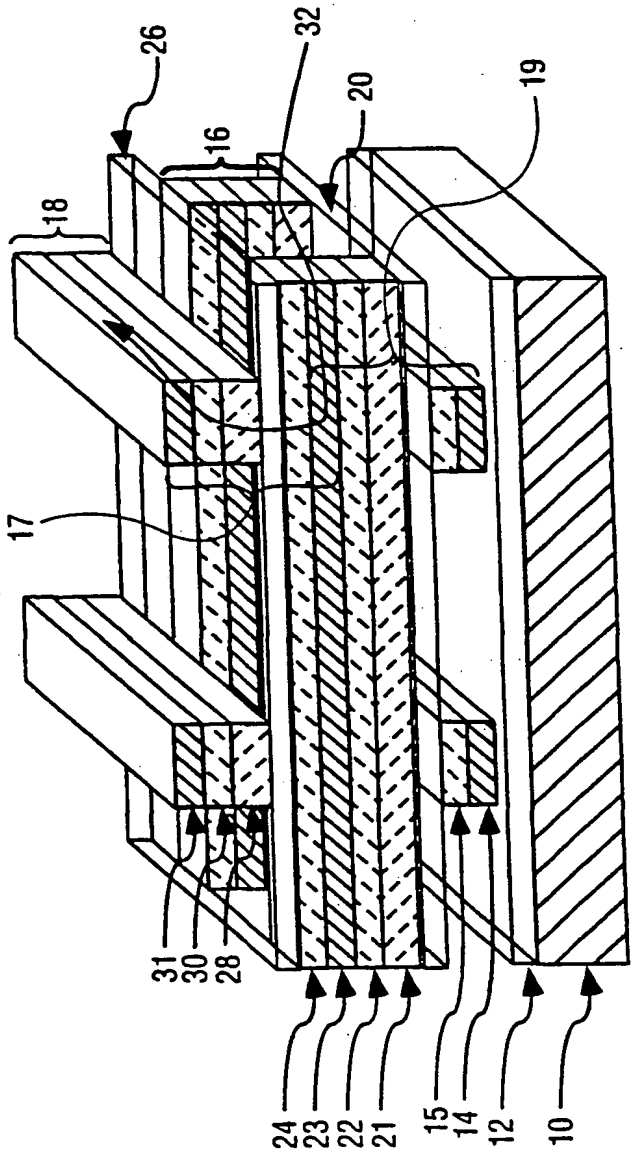


FIG. 1

FIG. 2A

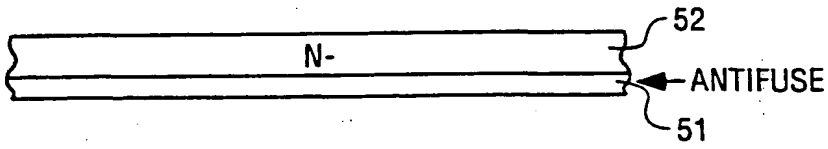


FIG. 2B

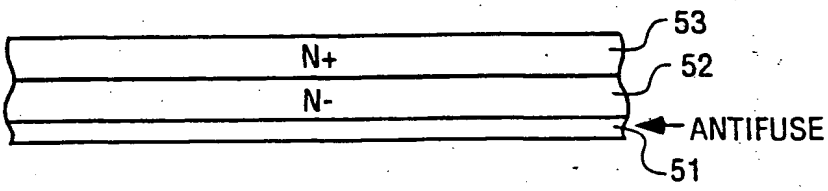


FIG. 2C

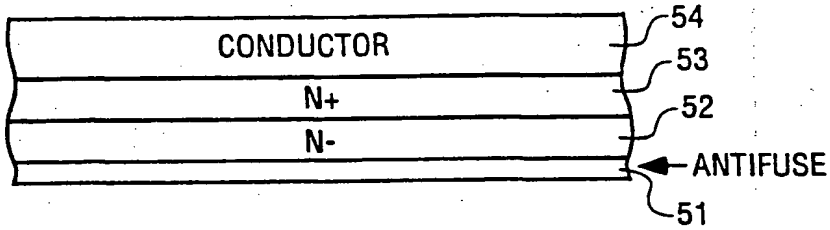


FIG. 2D

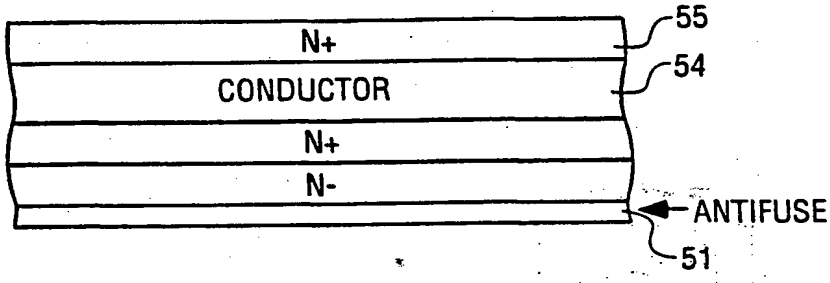
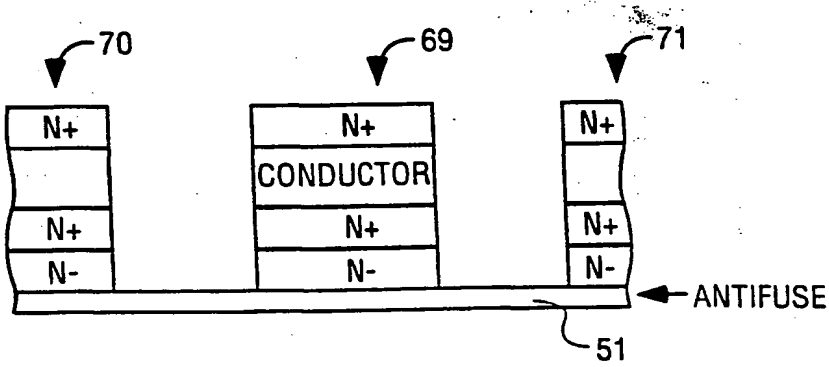


FIG. 2E



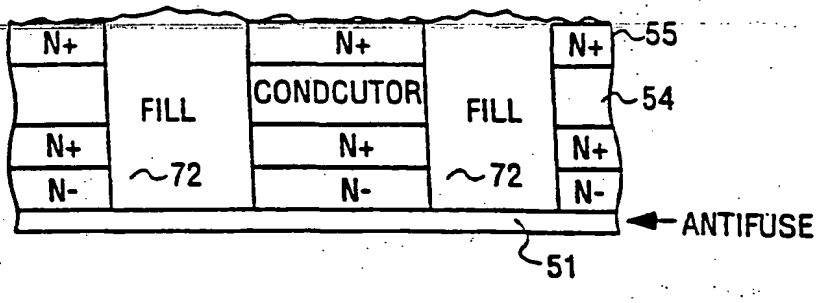


FIG. 2F

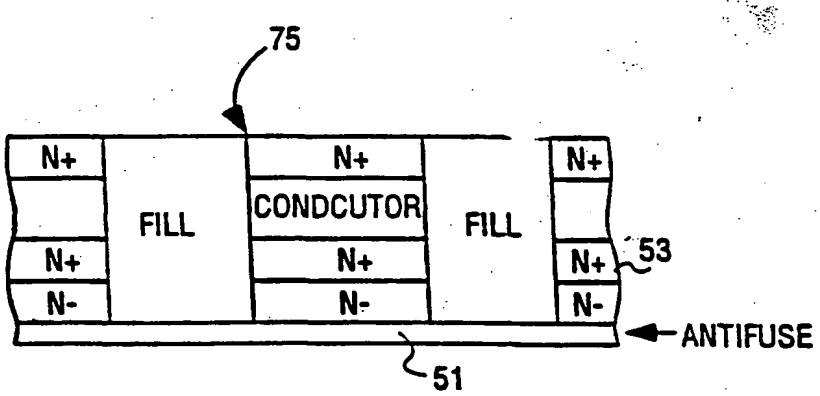


FIG. 2G

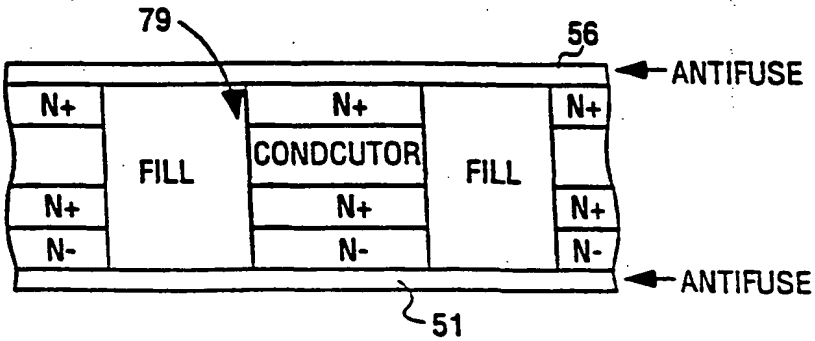


FIG. 2H

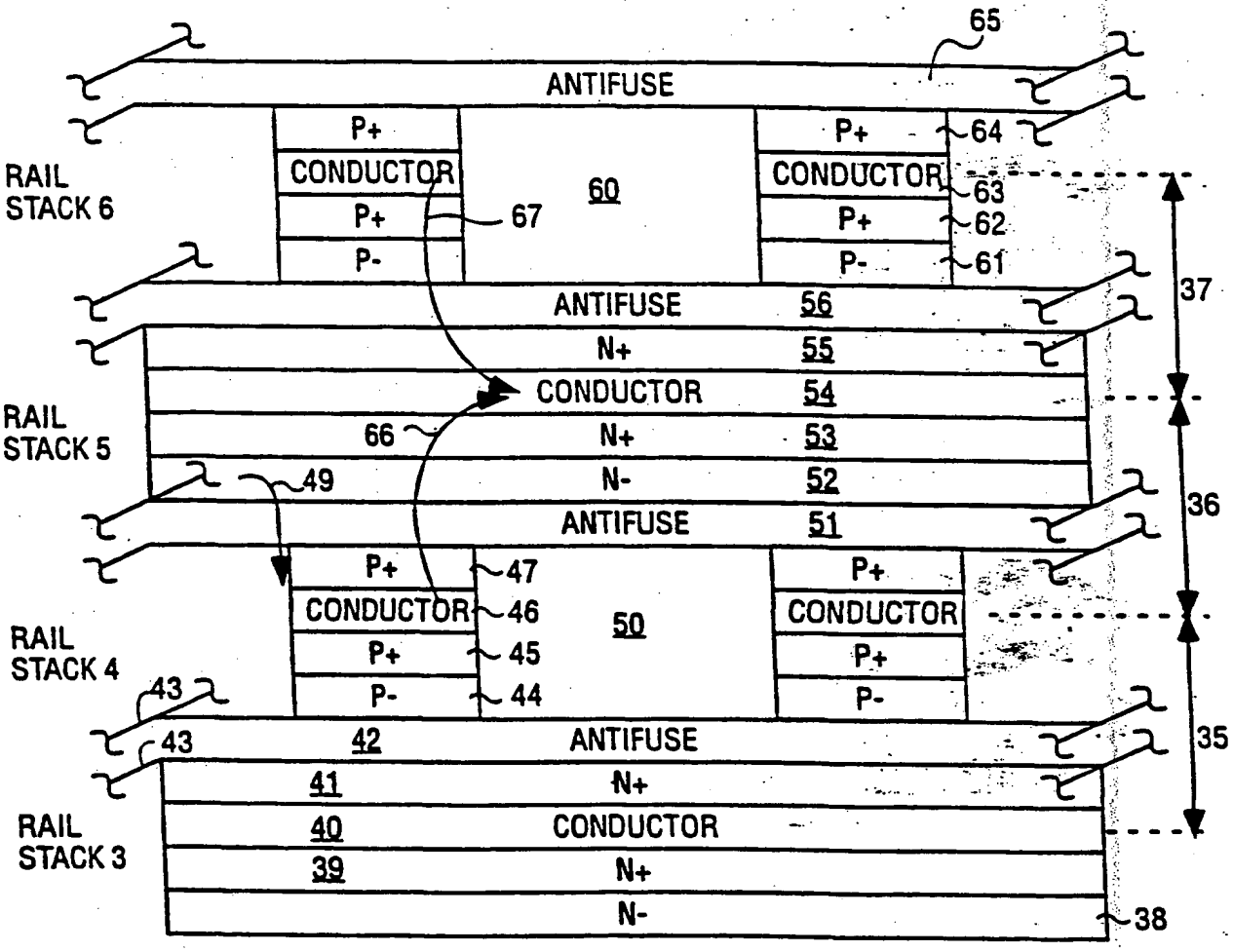


FIG. 3

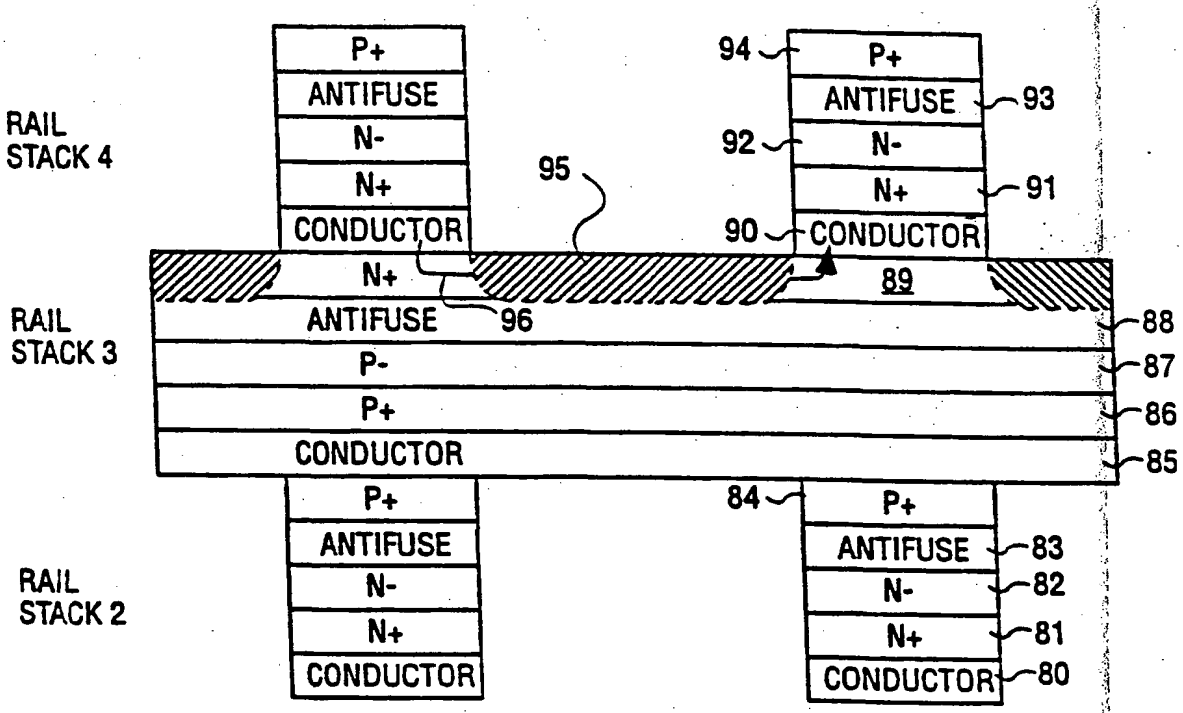

RAIL STACK 4
RAIL STACK 3
RAIL STACK 2
P+
ANTIFUSE
N-
N+
CONDUCTOR
95
94
92
93
91
90
89
96
88
87
86
85
84
83
82
81
80

FIG. 4

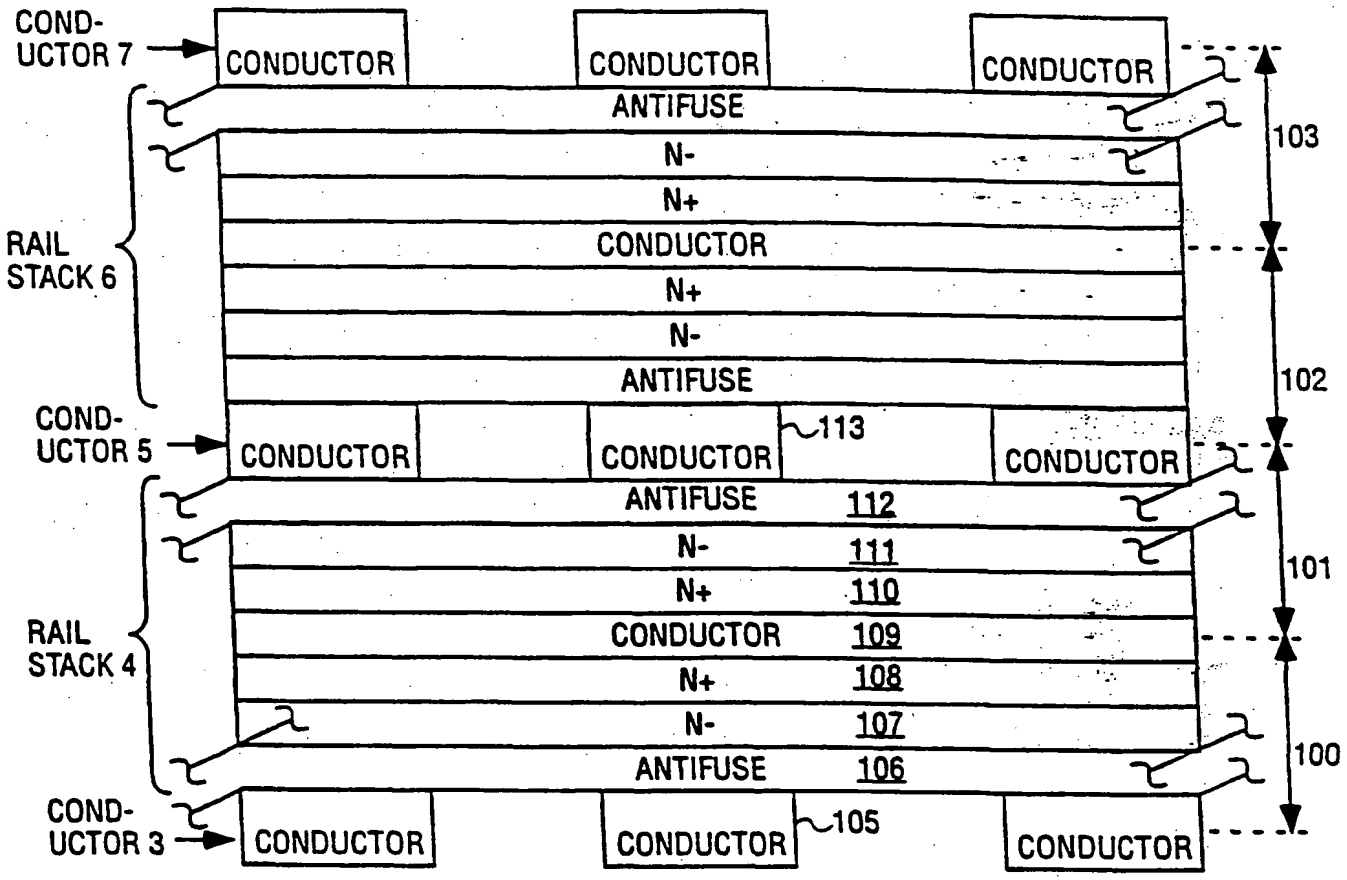


FIG. 5

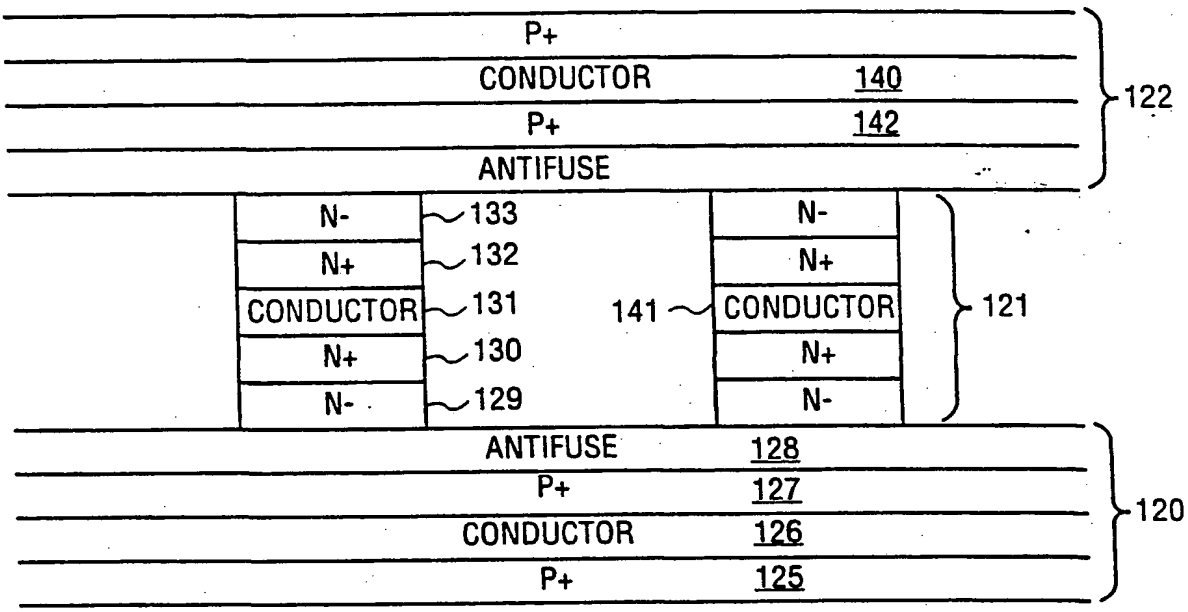


FIG. 6

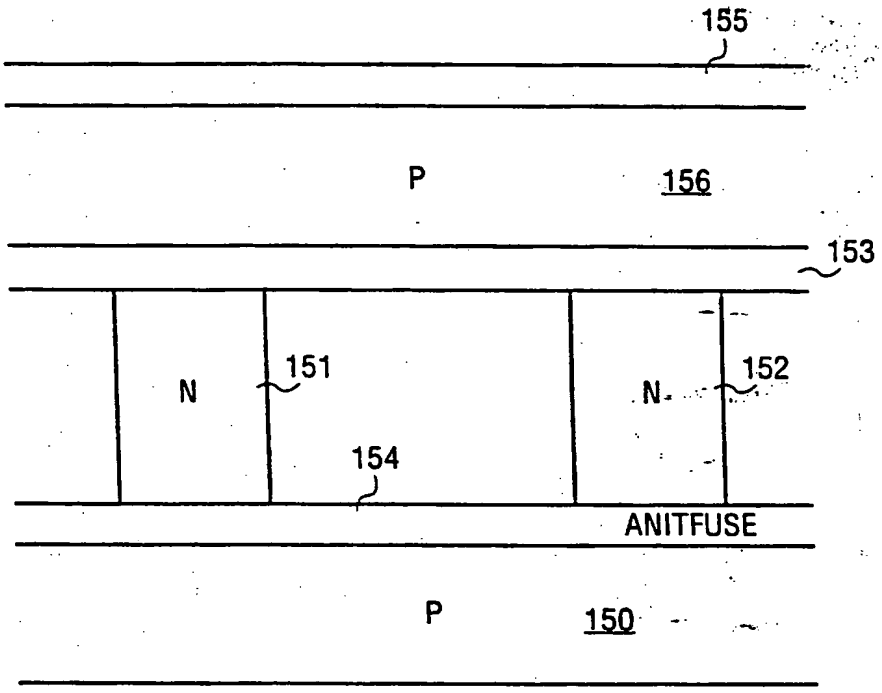


FIG. 7

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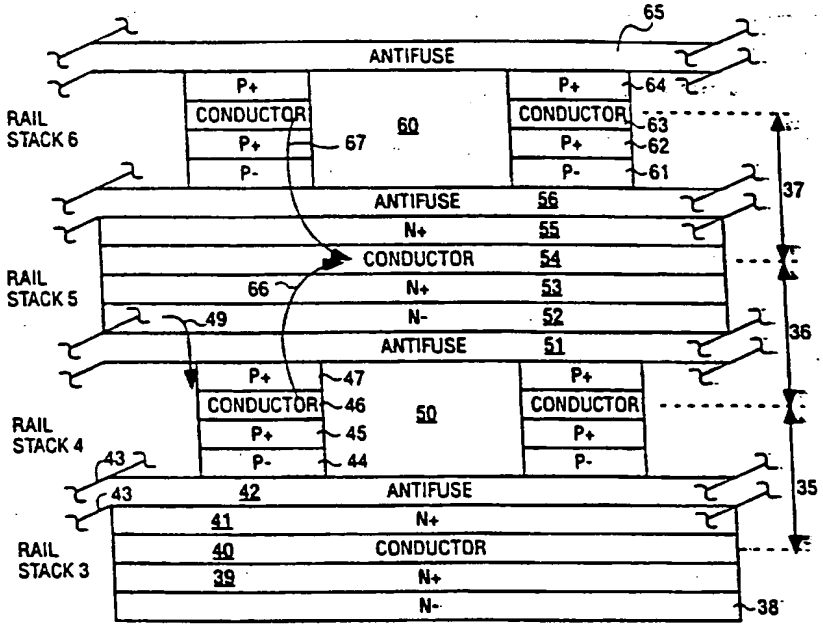
[Continued on next page]

(54) Title: THREE-DIMENSIONAL MEMORY ARRAY AND METHOD OF FABRICATION



(57) Abstract: A multi-level memory array is described employing rail-stacks. The rail-stacks include conductor (40) and semiconductor layers (38, 39 and 41). The layers are generally separated by an insulating layer used to form antifuses (42). In one embodiment, one-half the diode is located in one rail-stack and the other half in the other rail-stack. Methods for fabricating a multi-level memory array are also provided.

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A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 21/82

US CL :438/131

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/131, 128, 129, 130, 132; 365/225.7, 163, 168; 257/209, 798

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPAT, DERWENT, IBM Tech. Discl., EPOABS, JPOABS, US PGPubs

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4,646,266 A (OVSHINSKY et al.) 24 February 1987 (24.02.1987), see entire document.	1-111
A	US 5,991,225 A (FORBES et al.) 23 November 1999 (23.11.1999), see entire document.	1-111

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
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"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

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